Design limitations and its effect in the performance of ZC1-DPLL

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***Abstract*—The paper studies the dynamics of a conventional positive going zero crossing type digital phase locked loop (ZC1-DPLL) taking non-ideal responses of the loop constituent blocks into account. The finite width of the sampling pulses and the finite propagation delay of the loop subsystems are properly modeled mathematically and the system dynamics is found to change because of their influence considered separately. However, when these two are taken simultaneously, the system dynamics can be made nearly equivalent to that of the ideal system. Through an extensive numerical simulation a set of optimum parameters to overcome design limitations have been obtained.**

***Index Terms*—ZC1-DPLL, Delay, DCO Pulse Width, Bifurcation Diagram, Layapunov Exponent, Stability Zone, Convergence Time**

I. Introduction

Among different structures of digital phase locked loops (DPLLs) positive going zero crossing sampling type loops (ZC1-DPLLs) are widely used in practical applications [1,2,3,4]. In this DPLL, the input sinusoidal signal is sampled at the transition instants of the loop digitally controlled oscillator (DCO) signal and the DCO frequency is controlled by the filtered version of the sampled input signal. In the mathematical model of the ZC1-DPLL one makes a few approximations that are valid for an ideal system. For example, the width of the sampling pulses is taken to be infinitesimally narrow and as such the sampled voltages are considered as the instantaneous values at the sampling instants. Further, since the next sampling instant of the input signal is to be determined by the value of the sampled signal at the present instant, some processing has to be done on the sampled signal using physical circuits (viz, analog to digital converters, digital filters, DCO, etc.). Hence there would be a finite time delay in system response [5]. In mathematical modeling of the DPLL, this time delay is not considered.

In this paper our aim is to study the dynamics of a practical ZC1-DPLL without making these two approximations. Thus we treat the loop as a 'non-ideal' one. The finite width of the sampling pulse has been modeled by taking time averaged values of sampled signals in the duration of the sampled pulses and the finite propagation delay of the closed loop circuit is modeled by the inclusion of a pure phase delay network in the functional model of the loop. After deriving the system equation incorporating the abovementioned considerations, the dynamics of the practical ZC1-DPLL has been studied both numerically and quasi-analytically. Suitable design parameters have been assigned to take into account of the finite width of the sampling pulses (Δt) and nonzero loop time delay (τ). It has been observed that when the magnitudes of these become more than some critical values, the system dynamics becomes chaotic. Further these two effects have mutually opposite influence on the loop dynamics. From a different angle of view, we can point out that a controlled application of loop time delay or non-ideal finite width sampling pulses can provide us with predictable chaotic signal generators. These systems are of importance in chaos-based communication system design.

II. Derivation of system equation for non-ideal ZC1-DPLL

The functional block diagram of an ideal ZC1-DPLL is shown in Fig.1. It comprises of a sampler, a loop digital filter (LDF) and a digitally controlled oscillator (DCO).

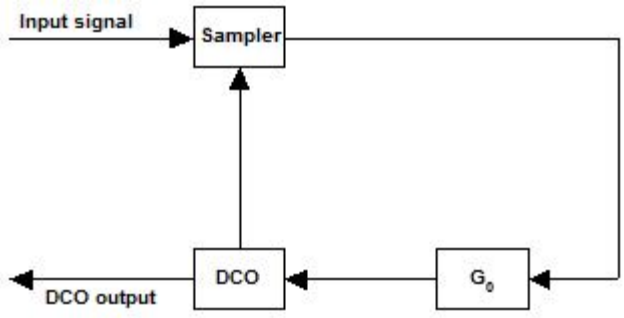

Fig. 1 Functional block diagram of ZC1-DPLL

For a non-ideal ZC1-DPLL we consider the width of sampling pulses as Δt and an over all loop propagation delay τ . The effect of the finite width of the sampling pulse would be felt at the output of the sampler. If the input signal to the sampler be,

$$x(t) = A_0 \sin(\omega_i t + \theta_0) \quad (1)$$

Where the noise free input signal $x(t)$ to have an angular frequency ω_i , amplitude A_0 and constant phase θ_0 . The sampled signal at the k^{th} sampling instant $t = t(k)$ $(k = 0,1,2.....)$ is written as $x(k)$ for an ideal DPLL as,

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$$x(k) = x(t(k)) = A_0 \sin(\omega_i t(k) + \theta_0) \quad (2)$$

However, for finite width sampling pulses the sampler output at the *k*-th sampled instant (SI) would be taken as a time average of $x(t)$ around $t(k)$ for a period Δt. Thus, sampled signal for a non-ideal DPLL would be given as $\overline{x(k)}$ where

$$\overline{x(k)} = \frac{1}{\Delta t} \int_{t(k)}^{t(k)+\Delta t} A_0 \sin(\omega_i t) dt \quad (3)$$

Normalizing the input signal frequency ω_i in terms of the DCO nominal frequency ω_o as, $\omega_i = \xi\omega_0$, and writing Δt in terms of the DCO nominal period T_0, $\Delta t = rT_0 = r(2\pi/\omega_0)$. One can write,

$$\overline{x(k)} = G_1 A_0 \sin[\omega_i t(k) + \xi\pi r] \quad (4)$$

Here we put, $G_1 = \frac{\sin(\xi\pi r)}{\xi\pi r}$. It is to be noted that the quantity G_1 accounts for the finite width of the sampling pulses through the parameter $r(=\Delta t/T_0)$. As r tends to zero would tend to one making the DPLL an ideal one.

Further it has been already mentioned that to analytically model an ideal ZC1_DPLL, the responses of the subsystems of a ZC1-DPLL (viz. sampler and quantizer, LDF and a DCO) have been considered to be instantaneous. But in practice, they will introduce a time delay, whatever small, in transmitting the signals through them and as such in the close loop response of the system one has to take into account an additional inherent time delay. This delay would definitely influence the dynamics of the loop. To derive the system equation of a delayed ZC1-DPLL the overall time delay has to be modeled by a suitable Z-domain transfer function. In the literature, a pure time delay (τ) is modeled in analog s-domain by the operator exp(-sτ), (s = jω). For a small delay, it can be approximated as,

$$e^{-s\tau} \cong \left(1 - \frac{s\tau}{2}\right) \Big/ \left(1 + \frac{s\tau}{2}\right) \quad (5)$$

Performing a bilinear transformation one can get the Z domain equivalent of the pure delay given in [5] as,

$$Z\left(e^{-s\tau}\right) = \frac{a + z^{-1}}{1 + az^{-1}} \quad (6)$$

Where *a* is a quantitative measure of the time delay, normalized to the sampling period of the digital system. Theoretically the parameter *a* can take values in the range $0 \le a \le 1$, but for simplified derivation of the system equation we may take the range as $0 < a \le 1$, where *a*= 0 indicates a delay of one sampling period and *a* = 1 indicates no delay. As expected, the delay network thus modeled gives unit amplitude gain and only pure phase shift, depending on the magnitude of *a*. The functional model of a "non-ideal" DPLL considered in this paper is shown in Fig.2. Here an average block (operating for an interval of sampling pulse width Δt) and a pure delay network have been included.

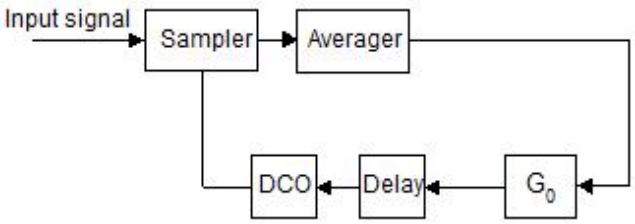

Fig. 2 Functional block diagram of delayed ZC1-DPLL

Now, the unmodulated and noise free input signal $x(t)$ to the loop is considered to have an angular frequency ω_i, amplitude A_0 and constant phase θ_0. The signal is written in terms of the DCO nominal frequency ω_0 as, $x(t) = A_0 \sin(\omega_0 t + \theta(t))$, where $\theta(t)$ is defined as $(\omega_i - \omega_0)t + \theta_0$. $x(t)$ is sampled at the instants determined by the DCO signal's positive going transition from one level to the other. The output of the LDF at the k^{th} SI denoted by $y(k)$ is used to control the period of the DCO according to the algorithm,

$$T(k+1) = T(k) - y(k)$$

Here $T_0 (= 2\pi / \omega_0)$ is the nominal period of the DCO and $T(k+1)$ is defined as the time elapsed between k^{th} and $(k+1)^{th}$ SI, i.e. $T(k+1) = t(k+1) - t(k)$. Considering $t(0) = 0$, one can write,

$$t(k) = kT - \sum_{0}^{k-1} y(i) \quad (7)$$

Now, considering the LDF as a gain element of magnitude G_0 and taking the pure time delay network into account one can write:

$$y(k) = \left[\frac{a + z^{-1}}{1 + az^{-1}}\right] G_0 x(k) \quad (8)$$

Here $x(k)$ stands for sampler output for an ideal ZC1-DPLL. The phase error between the input signal phase and the loop DCO phase is given by $\varphi(k)$ which is the signal angle at the sampling instant $t(k)$. Thus,

$$\varphi(k) = \omega_i t(k) + \theta_0$$

Using (7), one gets $\varphi(k)$

$$\varphi(k) = \omega_i t(k) + \theta_0 = \xi\omega_0 t(k) + \theta_0$$
$$= \xi k\omega_0 T_0 - \xi\omega_0 \sum_{i=0}^{k-2} y(i) + \theta_0 \quad (9)$$

Where, $\xi = (\omega/\omega_0)$. For an ideal ZC1-DPLL, the sampler output $x(k) = A_0 \sin\varphi(k)$, Now, after simple derivation of eqn.(9) using eqn.(8) one gets the phase governing equation as

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$$\varphi(k+2)=(1-a)\varphi(k+1)+a\varphi(k)+2\pi(1+a)(\xi-1)-$$
$$\xi K_0\left(a\sin\varphi(k+1)+\sin\varphi(k)\right) \quad (10)$$

Here ξ and K_0 have been substituted in place of (ω_i/ω_0) and $A_0\omega_0 G_0$.

Again due to consideration of finite width of sampling pulses the sampler output $x(k)$ must be replaced by $\overline{x(k)}$ in system equation derivation and after a simple algebra the system equation of the non-ideal system may be written as

$$\varphi(k+2)=(1-an)\varphi(k+1)+an\varphi(k)+2\pi(1+an)(\xi-1)-$$
$$\xi G_1 K_0\left(a\sin(\varphi(k+1)+\pi\xi r)+\{1+(n-1)a^2\}\sin(\varphi(k)+\pi\xi r)\right) \quad (11)$$

For a non-ideal DPLL, $n=1$ and for ideal DPLL $a=1$, $r=0$ and $n=0$.

III. Analytical calculation of stability zone of ZC1-DPLL with design limitations

The stability criterion of the non-ideal ZC1-DPLL can be obtained using the method outlined in the literature [7,8]. Define $\boldsymbol{X(k)}$ as a state vector given by $\boldsymbol{X(k)}=(\alpha(k),\beta(k))$, where $\alpha(k)$ and $\beta(k)$ are defined as $\alpha(k)=\varphi(k)$ and $\beta(k)=\varphi(k+1)$. If $\boldsymbol{X}^*$ is a value of $\boldsymbol{X}$ such that $\boldsymbol{X}=\mathrm{G}(\boldsymbol{X}^*)$. Then $\boldsymbol{X}^*$ is called fixed point of G, and under certain conditions, the sequence $\{\boldsymbol{X(k)}\}$ will converge to the solution $\boldsymbol{X}^*$, i.e., $\lim_{k\to\infty} X(k)=\boldsymbol{X}^*$. The Jacobian of the matrix is given by

$$J = G'\{X(k)\} = \begin{pmatrix} 0 & 1 \\ \eta & \rho \end{pmatrix} \quad (12)$$

Where, $\rho=(1-an)-aG_1\xi K_0\cos[\beta(k)+\pi\xi r]$ and $\eta=an-G_1\xi K_0\{1+(n-1)a^2\}\cos[\alpha(k)+\pi\xi r]$.

Now, for frequency step input $\xi\neq 1$. At the steady state $\varphi(k+2)=\varphi(k+1)=\varphi(k)=\varphi_{ss}$ (say), gives the steady state phase error as

$$\varphi_{ss}=\sin^{-1}\frac{2\pi(1+an)(\xi-1)}{\xi K_0 G_1\{1+a+(n-1)a^2\}}-\pi\xi r$$

For conventional DPLL, taking phase step input ($\xi=1$) the steady state phase error (φ_{ss}) is 0 (zero) whereas for non-ideal DPLL $\varphi_{ss}=-\pi\xi r$

Now considering this for $x^*=\varphi_{ss}$, equation (12) reduces to

$$\mathrm{G}(\mathrm{X}^*)=\begin{pmatrix} 0 & 1 \\ \eta_s & \rho_s \end{pmatrix} \quad (13)$$

Where we define the following quantities,

$$\eta_s=an-\sqrt{\left(\xi K_0 G_1\{1+a+(n-1)a^2\}\right)^2-\left(2\pi(1+an)(\xi-1)\right)^2},$$

$$\rho_s=(1-an)-a\sqrt{\left(\xi K_0 G_1\{1+a+(n-1)a^2\}\right)^2-\left(2\pi(1+an)(\xi-1)\right)^2}$$

Determining the eigen-values of the matrix (13) and applying the convergence condition [7], one gets the following stability condition

$$\frac{2\pi(1+an)(\xi-1)}{G_1\{1+a+(n-1)a^2\}}<K_0\xi<(1+an)\frac{\sqrt{(1+a)^2+(2\pi(\xi-1))^2}}{G_1\{1+a+(n-1)a^2\}} \quad (14)$$

Equation (14) reduces to that of an ideal DPLL for a=1, r=0 (i.e. G_i=1) and n=0 [7,8]. Thus keeping normalized input frequency (ξ) fixed, the phase locked condition could not be attained if the loop gain (K_0) be more than $\frac{\sqrt{(1+a)^2+(2\pi(\xi-1))^2}}{G_1\xi}$.

Again if keeping normalized input frequency (ξ) fixed, the phase locked condition could not be attained if the loop gain (K_0) be less than $2\pi(\xi-1)/G_1\xi$.

IVA. Numerical Simulation Results

The behaviors of the non-ideal ZC1- DPLL have been studied using the system equation (11). Fig. (3a) shows the bifurcation diagram of ideal ZC1-DPLL taking ξ = 1. Fig.s (3b), (3c) and (3d) show the bifurcation diagrams of non-ideal ZC1-DPLL for different values of design parameters (i.e. a and r) taking ξ = 1. From Fig.3b we have seen that for phase step input (ξ = 1) taking normalised delay parameter (a) =0.8 and normalised Sampling pulse width (r)=0 the phase locked condition could not be attained if the loop gain K_0 more than 1.72 and Fig.(3d) shows that for phase step input (ξ = 1) taking a=0.8 and r=0.2 the phase locked condition could not be attained if the loop gain K_0 more than 1.92 and Fig.(3c) shows that for phase step input (ξ = 1) taking a=1 and r=0.2 the phase locked condition could not be attained if the loop gain (K_0) greater than 2.2. The above results indicate that the upper limit of lock range increases due to increase of Sampling pulse width and decreases due to increase of loop time delay. Hence we may conclude that in a practical ZC1-DPLL circuit the upper limit of the lock range may remain almost unchanged as ideal ZC1-DPLL circuit for a suitable value of designing parameters a and r. It means that, although the presence of an additional delay reduces the stability zone of ZC1-DPLL, the finite pulse width increases the stability zone. Thus, a designer may make a trade-off between these two parameters to achieve an optimum loop operation. Fig.(5) shows this situation in the K_0- ξ space.

Fig. (6) shows the fastest convergence of ZC1-DPLL with design limitations taking different values of designing parameters (i.e. a and r). It can be found that for an ideal ZC1-DPLL, K_0=1 should be taken for fastest convergence. For a ZC1-DPLL with finite width of sampling pulses and for a delayed ZC1-DPLL the fastest convergence to a steady state can be achieved for K_0>1 and K_0<1, respectively and for non-ideal ZC1-DPLL (i.e. considering both design limitations) taking a=0.9 and r=0.2 the fastest convergence to a steady state can be achieved for K_0=1 and which is found in case of ideal ZC1-DPLL. It is also clear from the Fig.(6) that the effect on convergence time due to sampling pulse width and time delay oppose each other and for suitable values of parameters, a and r the overall effect may nullifies each other.

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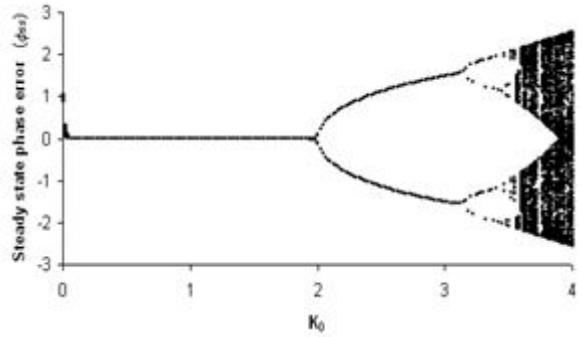


Fig.3a Bifurcation diagram, plotting steady state phase error φ_{ss} (rad) with different loop gain (K_0) for an ideal ZC1-DPLL (i.e., r=0, a=1 and n=0) at ξ = 1

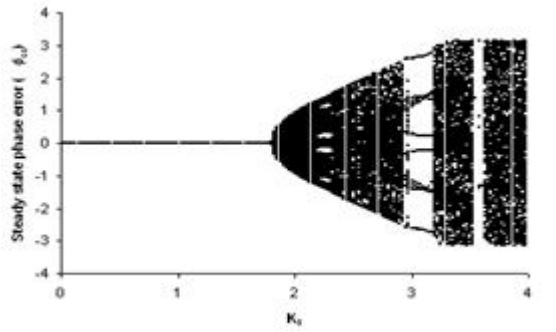


Fig.3b Bifurcation diagram of φ_{ss} (rad) with different loop gain (K_0) for an *non-deal* ZC1-DPLL having inherent time-delay a=0.8 (with r=0 and n=1) at ξ = 1

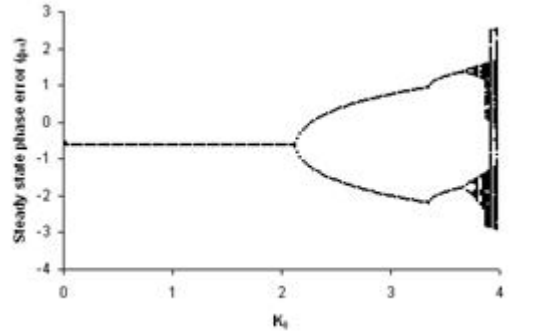


Fig.3c Bifurcation diagram of φ_{ss} (rad) with different loop gain (K_0) for an *non-deal* ZC1-DPLL having finite pulse width (r=0.2); (with a=1 and n=1) at ξ = 1

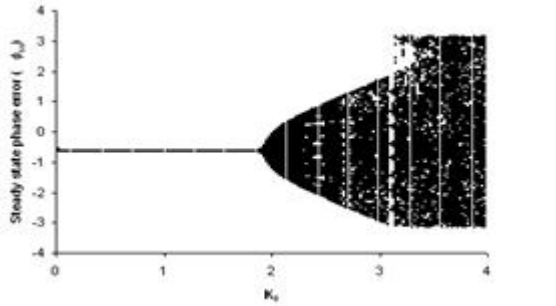
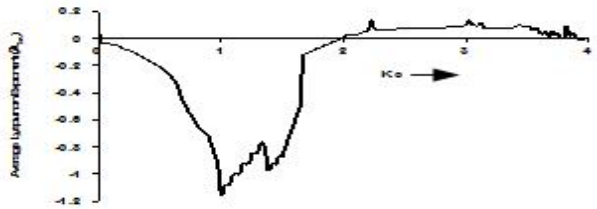


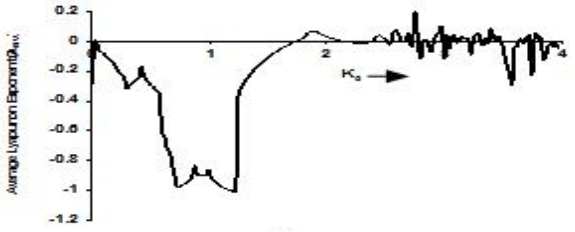
Fig.3d Bifurcation diagram of φ_{ss} (rad) with different loop gain (K_0) for an *non-deal* ZC1-DPLL (i.e. n=1) having inherent time-delay (a=0.8) and finite pulse width (r=0.2) at ξ = 1

IVB. Time Series Analysis

The occurrence of chaos in a dynamical system can be qualitatively measured by computing average Lyapunov exponent. Lyapunov exponents quantify the exponential divergence of initially close state-space trajectories and estimate the amount of chaos in a system. A positive Lyapunov exponent indicates chaos and in this situation the system will be very sensitive to initial conditions. The techniques of calculation of Lyapunov exponent from time series data of a system variable is well documented in literature [9,10]. We calculate the Lyapunov exponent of ideal ZC1-DPLL and non-ideal ZC1-DPLL from time series data of phase errors with different loop gain values K_0 (for phase step input, i.e. ξ = 1). Fig. (4a), (4b), (4c) and (4d) show the Lyapunov Exponent of ZC1-DPLL for different values of designing parameters (i.e. a and r) with ξ = 1. Fig.(4b) shows that taking a=0.8 and r=0 the average Lyapunov exponent is negative as the controlled parameter K_0 is varied from 0 to 1.72 and Fig. (4d) shows that for a=0.8 and r=0.2 the average Lyapunov exponent is negative as the controlled parameter K_0 is varied from 0 to 1.92 and the same result also has been found analytically. Fig. (4c) shows that taking loop delay parameter a=1 and normalized sampling pulse width r=0.2 the average Lyapunov exponent is negative as the controlled parameter K_0 is varied from 0 to 2.2. From Fig. (4b) and Fig. (4d) we conclude that the reduction of steady state phase error zone due to loop time delay is more or less compensated due to increase of sampling pulse width. Here we may conclude that the results found related to steady state zone using Lyapunov exponent agree with the results found from bifurcation diagrams and analytical predictions.



(a)



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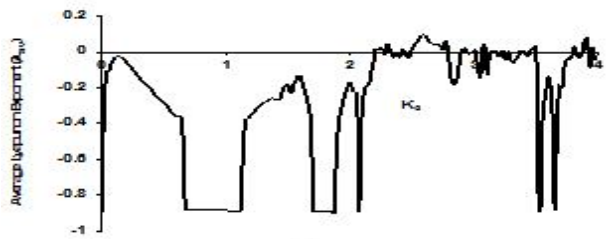

(c)

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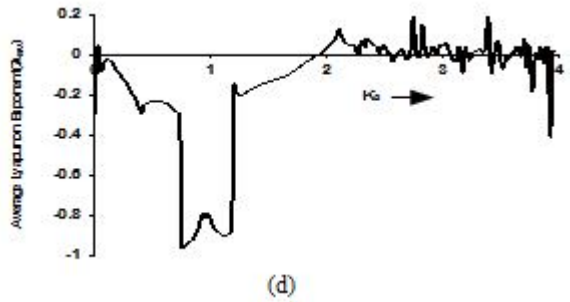

Fig. 4d Plotting of average Lyapunov Exponent (λ_{av}) with different values of loop gain K_0 for (a) ideal ZC1-DPLL (b) a=0.8, r=0 (c) a=1, r=0.2 (d) a=0.8, r=0.2 (ξ = 1)

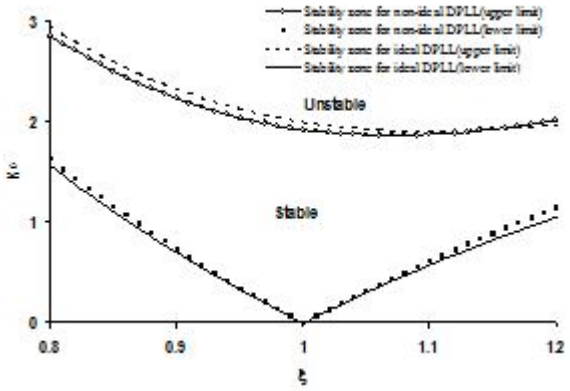

Fig. 5 Stability zone for ideal ZC1-DPLL and non-ideal DPLL with values of design limitations parameter a=0.8, r=0.2

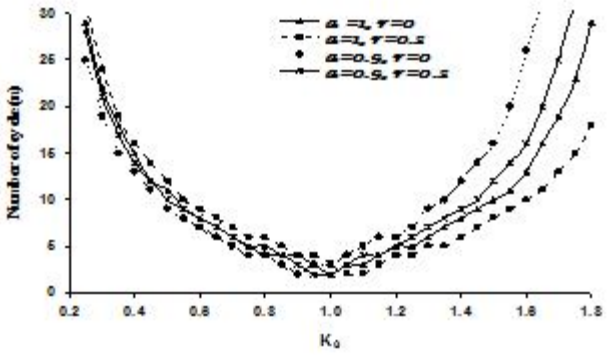

Fig. 6 Plotting of convergence time (in number of cycle) with different values of loop gain K_0 for ideal ZC1-DPLL and ZC1-DPLL with finite width of sampling pulses

V. Conclusions

This paper reports the effect of loop time delay and finite sampling pulse width on the dynamical behavior of a ZC1-DPLL. For an ideal ZC1-DPLL one considers that there would be no additional loop time delay and also the width of sampling pulses are narrow enough. But in a practical system there is always an additional time delay in the loop and also the sampling pulses are not instantaneous but they have a finite width. These two effects should have to be considered to explore the complete dynamical behavior of a ZC1-DPLL. The stability of the loop has been found to be affected by the loop time delay and finite width of sampling pulse. Further using nonlinear dynamical loops like bifurcation diagram (local) and time series analysis it has been shown that the loop dynamics shows period doubling bifurcation and chaos for the variation of loop time delay and sampling pulse width. The authors believe that the present study would help the designers to design optimum practical DPLL where the practical design limitations (such as loop time delay and Δt) have been considered.

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